Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended) An integrated circuit, comprising:

a first transistor;

an analog-to-digital converter ~~coupled to the first transistor~~ comprising comparators that compare a voltage at a terminal of the first transistor to a series of resistance values, wherein a first set of the comparators generates HIGH output signals and a second set of the comparators generates LOW output signals in response to the voltage at the terminal of the first transistor;

a digital encoder circuit coupled to receive ~~output signals of the analog-to-digital converter~~ the output signals of the comparators, the digital encoder encoding the output signals of the comparators into digital signals that represent a binary value, the binary value indicating how many of the comparators generate the HIGH output signals; and

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an impedance matching circuit coupled to receive output signals of the digital encoder circuit~~, the digital encoder output signals characterized by values~~, wherein the impedance matching circuit comprises a plurality of second transistors coupled in parallel~~, wherein an impedance of the impedance matching circuit increases in response to a change in the values of the digital encoder output signals in a first direction and wherein the impedance of the impedance matching circuit decreases in response to a change in the values of the digital encoder output signals in a second direction~~.

Claim 2. (original) The integrated circuit of claim 1 wherein the first transistor is coupled to a resistor.

Claim 3. (original) The integrated circuit of claim 1 wherein the impedance matching circuit is coupled in parallel with an I/O pin of the integrated circuit.

Claim 4. (original) The integrated circuit of claim 1 wherein the impedance matching circuit is coupled in series with an I/O pin of the integrated circuit.

Claim 5. (original) The integrated circuit of claim 4 wherein the impedance matching circuit is coupled to a buffer circuit that is coupled to the I/O pin.

B' cont'd

Claim 6. (original) The integrated circuit of claim 1 further comprising a plurality of impedance matching circuits coupled to receive output signals of the digital encoder circuit, wherein the plurality of impedance matching circuits each comprises a plurality of transistors coupled in parallel.

Claim 7. (canceled)

Claim 8. (currently amended) The integrated circuit of claim ~~7~~ 1 wherein the analog-to-digital converter comprises a plurality of resistors that set threshold voltages for the plurality of comparators.

Claim 9. (original) The integrated circuit of claim 1 wherein the plurality of second transistors of the impedance matching circuit comprises four transistors coupled in parallel.

Claim 10. (original) The integrated circuit of claim 1 wherein the plurality of second transistors of the impedance matching circuit comprises five transistors coupled in parallel.

Claim 11. (currently amended) A method for providing impedance matching to a pin of an integrated circuit using an impedance matching circuit, the method comprising:

generating a first signal in response to an impedance of a first transistor;

comparing a voltage at a terminal of the first transistor to a plurality of resistances using comparators, wherein a first set of the comparators generates HIGH output signals and a second set of the comparators generates LOW output signals in response to the voltage;

~~converting the first signal into a plurality of second signals~~ encoding the output signals of the comparators into digital signals that represent a binary value, the binary value indicating how many of the comparators generate the HIGH output signals; and

setting an impedance of the impedance matching circuit in response to the ~~plurality of second~~ digital signals, wherein the impedance matching circuit is part of the integrated circuit ~~and the impedance of the impedance matching circuit increases in response to a first condition of the plurality of second signals and decreases in response to a second condition of the plurality of second signals~~.

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Claim 12. (original) The method of claim 11 wherein generating the first signal comprises generating the first signal from a resistor divider circuit that comprises the first transistor and a resistor.

Claim 13. (currently amended) The method of claim 11 wherein ~~converting the first signal in to a plurality of second signals comprises converting the first signal into a plurality of digital signals using an analog-to-digital converter~~ the comparators include at least 15 comparators.

Claim 14. (currently amended) The method of claim 13 wherein ~~converting the first signal in to a plurality of second signals further comprises converting the plurality of digital signals into the plurality of second signals using a digital encoder circuit, wherein the plurality of second signals is fewer in number than the plurality of~~

~~digital signals~~ encoding the output signals of the comparators into digital signals that represent the binary value further comprises encoding the comparator output signals into 4 digital signals.

Claim 15. (currently amended) The method of claim 14 wherein ~~the digital encoder circuit converts the digital signals into the plurality of second signals that are a binary bit representation of the digital signals~~ encoding the output signals of the comparators into digital signals that represent the binary value further comprises performing Boolean NAND functions on the output signals of the comparators.

Claim 16. (currently amended) The method of claim 11 wherein setting the impedance of the impedance matching circuit further comprises causing each one of a plurality of second transistors to be ON or OFF in response to the ~~plurality of second~~ digital signals.

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Claim 17. (original) The method of claim 16 wherein the plurality of second transistors comprises at least four transistors coupled in parallel.

Claim 18. (original) The method of claim 11 wherein the impedance matching circuit comprises at least five transistors coupled in parallel.

Claim 19. (original) The method of claim 11 wherein setting the impedance of the impedance matching circuit further comprises setting the impedance of a plurality of impedance matching circuits wherein each one of the plurality of impedance matching circuits comprises a plurality of transistors coupled in parallel.

Claim 20. (currently amended) The method of claim 19 wherein ~~the plurality of~~ a subset of the impedance matching circuits are coupled ~~in series or~~ in parallel with respect to an associated I/O pin of the integrated circuit.

Claim 21. (currently amended) An integrated circuit comprising:

programmable logic circuitry;

a first transistor for generating an analog signal;

~~circuitry for generating a plurality of digital signals in response to the analog signal, wherein the circuitry includes an analog-to-digital converter, and the digital signals comprise a binary representation of the analog signal~~

an analog-to-digital converter comprising comparators that compare the analog signal to resistance values, wherein each of the comparators generates a HIGH or LOW output signal in response to the analog signal;

a digital encoder circuit coupled to the analog-to-digital converter, the digital encoder encoding the output signals of the comparators into digital signals that represent a binary value, the binary value indicating how many of the comparators generate the HIGH output signals; and

13' cont'd

an impedance matching circuit comprising a plurality of second transistors, wherein each of the second transistors is coupled to receive one of the digital signals~~, wherein a first state of the digital signals results in an increase in a resistance of the impedance matching circuit and a second state of the digital signals results in a decrease in the resistance of the impedance matching circuit~~.

Claim 22. (original) The integrated circuit of claim 21 further comprising a plurality of impedance matching circuits, each comprising a plurality of transistors that are each coupled to receive one of the digital signals.

Claim 23. (original) The integrated circuit of claim 22 wherein each of the impedance matching circuits are associated with an I/O pin of the integrated circuit.

Claim 24. (original) The integrated circuit of claim 23 wherein a subset of the impedance matching circuits are coupled to a buffer circuit.

Claim 25. (original) The integrated circuit of claim 23 wherein a subset of the impedance matching circuits are coupled in parallel with an associated one of the I/O pins.

Claim 26. (currently amended) The integrated circuit of claim 21 wherein the ~~circuitry further comprises a digital encoder circuit coupled to the analog-to-digital converter~~ the digital encoder circuit further comprises a plurality of NAND gates and NOR gates.

B' cont'd

Claim 27. (original) The integrated circuit of claim 21 wherein the first transistor is coupled to an off-chip resistor, and wherein the first transistor and the off-chip resistor form a resistor divider.

Claim 28. (original) The integrated circuit of claim 21 wherein the plurality of second transistors comprises at least four transistors coupled in parallel.